

Flashlite 386EX

User's Manual

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Overview

The Flashlite 386Ex single board computer is based on the Intel 386Ex microcomputer. The 386Ex is a high performance, 32-bit, single-chip microcomputer that is software compatible with the Intel 80386 family of microprocessors. DOS compatibility allows development in a familiar environment with a wide range of tools. High endurance flash memory eliminates EPROM programming without worry of damaging the onboard non-volatile memory with repeated program cycles. Applications are uploaded directly into the flash disk. Expansion options provide high capacity flash storage eliminating the size and reliability problems associated with electro-mechanical storage devices.

Software development for the Flashlite is remarkably simple and quick. Programs are written on a PC compatible computer in the language of your choice. After your application has been compiled or assembled and linked into .EXE or .COM form, it is uploaded to the Flashlite's flash disk with your favorite telecommunications program using the X-Modem protocol. The application can then be tested and debugged through the console serial port. When the application is running to your satisfaction, the startup batch file can be modified so that the application will load and execute upon reset or powerup.

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Features

- 25MHz Intel 386Ex Processor
- 256k / 512k Bytes SRAM Memory
- 512k Bytes Flash Memory
- High Speed PC Compatible Serial Ports:
 - 1 Full-Function (8-wire) RS-232 Port
 - 1 Software Configurable as 3-wire RS-232 or RS-485
- Synchronous 4-Wire Serial Port
- 3 PC Compatible Counter/Timers
- Hardware Watchdog
- 36 Digital I/O Lines
- 2 Enhanced DMA Channels
- Clock Calendar
- 32Pin Dip Socket to accept 512k x 8 bit SRAM, 512k x 8 bit Flash, or M-Systems DiskOnChip 2000.
- High-Efficiency Switching Power Supply (7-34V DC Input)
- Full Address/Data Expansion Bus

Operation

The Flashlite 386Ex is configured with two 'disk drives' A: and B:. Drive A: contains the operating system, the BIOS, and utility programs essential to the operation of the Flashlite. Drive A: is read-only. Drive B: is read/write and contains optional utility programs and is available for user files and applications.

The serial port commonly known as COM2 on the PC is the console for the Flashlite. The port is configured for 9600 baud, 8 data bits, 1 stop bit and no parity. This is the primary mode of communicating with the Flashlite. DOS and the BIOS treat the console port as the logical devices STDIN and STDOUT. The second port is addressed and assigned interrupt vectors the same as COM1 on a PC.

When power is applied to the Flashlite or when it is reset, the board goes through its initialization procedure and then starts DOS. A simple `AUTOEXEC.BAT` file is executed and then the board is ready to use. The batch file performs several functions before the user is given control. The DOS search path is set, the DOS prompt is set, the CNTL-C flag (discussed later in this manual) is checked and finally, an attempt is made to execute a file named `STARTUP` on the B: drive. This provides a convenient way for custom applications to execute immediately after initialization of the Flashlite. If you wish to have your application start automatically, create a batch file named `STARTUP.BAT` that invokes the program. It is possible, but not recommended, to rename your application `STARTUP.EXE` or `STARTUP.COM`. If this is done and the program locks up, typing CNTL-C at bootup may not break the program and exit to the DOS prompt.



Although the flash memory devices used have a guaranteed lifetime of over 10,000 write cycles, it is possible for an application to quickly wear them out. The flash memory is intended to store programs and setup data which are normally not changed. Avoid storing data or frequently changed information on the flash disk.

Getting Started

To begin development with the Flashlite, you will need a PC compatible computer with a telecommunications program and a free serial port. Connect the Flashlite's connector J11 to the PC's serial port with a 9-pin ribbon cable, PN 86-0000. Run the telecommunications program and configure the serial port for 9600 baud, 8 data bits, 1 stop bit and no parity. Hardware and Software Handshaking are not required. Apply power to the Flashlite, using our A/C adapter PN 88-0005 or a source of unregulated DC between 7 and 34 volts, capable of supplying 2 Watts. J1 pin 1 or J4 pin 1 (square pad on bottom of board) is positive.

The Flashlite should respond with a welcome message and a B: prompt. Enter DIR to look at the directory of drive B:. If you do not get a welcome message or characters that you type do not echo, you need to check your serial port setup. To test everything but the Flashlite, remove the serial cable from J11 and jumper pins 3 and 5 with a wire or paper clip. If characters typed on the keyboard are not echoed on the screen, the problem is with your setup. You must resolve the problem before you can continue.

If you were able to do a DIR, take a few minutes to explore the contents of the Flashlite's file system. You will find all of the essential utilities on drive A: and some optional programs on drive B:. Drive A: is write-protected and cannot be altered. Drive B: is read/write and can be changed or reformatted.

After you have looked at the programs on the Flashlite, the next step is to try to upload a file. This is the procedure for getting a file from your PC to the Flashlite. On the Flashlite, type the command UP followed by the name of the file you wish to upload. The Flashlite will begin sending characters to your PC polling it for the file.

On your PC, start the transfer, usually by pressing the PgUp key. The telecomm program should respond by requesting the file name and protocol. Enter the file name and select X-Modem for the protocol. The transfer should start and when it is complete, you should get a new B: prompt on the screen. If the transfer does not work, the problem is most likely the Carrier Detect signal (pin 1 on the DB-9 connector) into the PC being sensed as low or false. Make sure that the signal is at least +3 volts into your PC if you are not able to transfer files.

If the transfer terminated without problems, you have a working development environment for the Flashlite controller. At this point, you may wish to download the files EDIT.COM and BASIC.COM from the Flashlite to your PC. Start the download on the Flashlite by typing DOWN BASIC.COM and pressing Enter.

Getting Started

On your PC, begin the transfer, usually by pressing PgDn. After the file is transferred, repeat the process with `EDIT.COM`. These files are also found on the JK microsystems web site.

The Flashlite has a hardware clock calendar. Time and date can be set with the following commands:

```
B:\>TIME 13:30:00      Sets the time to 1:30 pm
B:\>DATE 11-19-99      Sets the date to November 19, 1999
```

When power is applied to the Flashlite, one of the first things the BIOS initialization code does is check for a CNTL-C character typed at the console. If this character is typed as soon as the board is powered up or reset, a flag is set which overrides the quiet state of the console (discussed below). When DOS runs its `AUTOEXEC.BAT` file on drive A:, the state of the CNTL-C flag is also checked and any user application set to run on drive B: is not loaded. This insures that a hung application or quiet console can always be interrupted.

If the CNTL-C flag is not set, the `AUTOEXEC` file will attempt to transfer control to a file named `STARTUP` on drive B:. DOS also looks for and, if present, loads `CONFIG.SYS` from drive B:.

The Flashlite console output and input can be controlled using the `QUIET` and `NOQUIET` commands. This is useful for applications where both serial ports must talk to hardware devices without disturbance from console messages.

Running `QUIET` will turn off both input and output on the console port, allowing applications to use it as COM2. Pressing CNTL-C immediately after reset or powerup will restore the console until the next reboot. Running `NOQUIET` will restore the default setting of an active console. `QUIET` modifies a byte in the BIOS Flash data area and will take effect after the board is reset. If you need to toggle the state of the console while an application is running, a one can be written to the byte at 40:8B (BIOS RAM Data) to disable the console or a zero can be written to enable the console. Changes to the quiet flag stored in RAM will not change the state of the flag in Flash and may not be valid after a reset.



A Flashlite in quiet mode may appear to be non-functional. When troubleshooting a system, always try pressing CNTL-C while applying power.

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Hardware

Memory Configuration

The 386Ex processor is initially configured in real mode with a physical address space of 1 megabyte. The SRAM is located between 00000h and 7FFFFh, the flash is between 80000h and FFFFFh. A 32-pin DIP socket is provided for additional flash, RAM, or EPROM data. This memory can be accessed by reprogramming the chip select unit in the 386Ex or by entering protected mode.

I/O Configuration

The 386Ex is configured for enhanced DOS mode. This mode provides access to the PC/AT peripherals such as UARTs, counter/timers, and the interrupt controller at their traditional I/O port addresses. Other 386Ex peripherals are accessible in expanded I/O space.

For addressing and programming the peripherals specific to the 386Ex, please refer to the Intel 386Ex Embedded Microprocessor User's Manual (Intel document number 272485-002). The manual is available in PDF format from our web site at <http://www.jkmicro.com>

Digital I/O Ports

The Flashlite has six I/O ports controlling a total of 36 bits of I/O. The ports are configured in groups as described below.

Signals on Ports A,B and C are generated by an 82C55 general purpose programmable I/O device. A word of caution, any time the 82C55 control register is written to, any output bit that is in the ON state will be turned OFF. This is a feature of the silicon aimed at protecting outputs from driving unknown loads that could possibly damage the chip. Ports D and E are generated by a programmable logic chip. Ports F and G are I/O pins on the 386Ex processor.

NOTE: Be careful to change only the required bits when working with the I/O ports. Some pins are used to control other on-board functions that can be reprogrammed or disabled through these configuration registers. Refer to the chip datasheets for more information on configuring these ports.

Port A, I/O Address 60 Hex

Bit	7	6	5	4	3	2	1	0
Name	PA.7	PA.6	PA.5	PA.4	PA.3	PA.2	PA.1	PA.0
Default	IN	IN	IN	IN	IN	IN	IN	IN
Pin	J2-11	J2-13	J2-15	J2-17	J2-19	J2-21	J2-23	J2-25

Port A is located at I/O address 60 hex and is configured as a group as either inputs or outputs. The default configuration is inputs. To make all bits output, set bit 4 of I/O address 63 hex to a zero, preserving the state of the other bits.

Port B, I/O Address 61 Hex

Bit	7	6	5	4	3	2	1	0
Name	PB.7	PB.6	PB.5	PB.4	PB.3	PB.2	PB.1	PB.0
Default	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
Pin	J2-12	J2-14	J2-16	J2-18	J2-20	J2-22	J2-24	J2-26

Port B is located at I/O address 61 hex and is configured as a group of either inputs or outputs. The default configuration is outputs. To make all bits input, set bit 1 of I/O address 63 hex to a one, preserving the state of the other bits.

Note: PB.1 is used to gate the PC speaker output. The speaker output may not be used when PB.1 is controlled by the user program.

Port C, I/O Address 62 Hex

Bit	7	6	5	4	3	2	1	0
Name	PC.7	PC.6	PC.5	PC.4	PC.3	PC.2	PC.1	PC.0
Default	OUT	OUT	OUT	OUT	IN	IN	IN	IN
Pin	J14-5	J14-7	J14-9	J14-11	J14-18	J14-17	J14-20	J14-19

Port C is located at I/O address 62 hex and is configured as 2 groups of 4 bits each. The default configuration for bits PC.0 to PC.3 is inputs. To make these bits outputs, set bit 0 of I/O address 63 hex to a zero.

The default configuration for bits PC.4 to PC.7 is outputs. To make these bits inputs, set bit 3 of I/O address 63 hex to a one. When reconfiguring the I/O status of these pins, be sure to preserve the state of the other bits.

Port D, I/O address FA02 hex

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	PD.3	PD.2	PD.1	PD.0
Default	-	-	-	-	IN	IN	IN	IN
Pin	-	-	-	-	J7-4	J7-3	J7-2	J7-1

Port D is located at I/O address FA02 hex and is configured as a group as either input or output. The default configuration of Port D is input. To configure Port D as outputs, set bit 0 of I/O address FA00 hex to a one.

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Port E, I/O Address FA03 Hex

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	PE.3	PE.2	PE.1	PE.0
Default	-	-	-	-	IN	IN	IN	IN
Pin	-	-	-	-	J7-8	J7-7	J7-6	J7-5

Port E is located at I/O address FA03 hex and is configured in three groups. The default configuration is input. To configure PE.0 and PE.1 as output, set bit 1 of I/O address FA00 to a one. To configure PE.2 as an output, set bit 2 of I/O address FA00 to a one. To configure PE.3 as an output, set bit 3 of I/O address FA00 to a one. In each case, be sure to preserve the other bit settings.

Port F, I/O Address F860 and F862 Hex

Bit	7	6	5	4	3	2	1	0
Name	PF.7	PF.6	PF.5	PF.4	-	-	-	-
Default	IN	IN	IN	IN	-	-	-	-
Pin	J12-4	J12-3	J12-2	J12-1	-	-	-	-

The data on Port F can be read by inputting I/O address F860 hex. The default configuration is input. Each bit of Port F can be individually configured for input or output. To configure a bit for output, write a zero in that bit position to I/O address F864 hex. To output data on Port F, write the data to address F862 hex.

P1PIN: F860h, Port Pin Status Register (read only), bits 4-7

P1LTC: F862h, Port Latch Register, bits 4-7

P1DIR: F864h, Port Direction Register, bits 4-7, 0 for output, 1 for input or open drain output.

P1CFG: F820h, Port Configuration Register, bits 4-7 low, route P1.4-P1.7 to chip pins (BIOS Default)

Port G, I/O Address F870 and F872 Hex

Bit	7	6	5	4	3	2	1	0
Name	-	-	PG.5 EXFLAG	PG.4 IRQ6	PG.3 IRQ5	PG.2 PCFLAG	PG.1 IRQ3	PG.0 IRQ4
Default	-	-	IN	IN	OUT	IN	IN	IN
Pin	-	-	J10.8	J12-8	J12.7	J10.19	J13.15	J13.17

The data on Port 3 can be read from I/O address F870 hex. The default pin direction is shown above. Each bit of Port 3 can be individually configured as an input or output. To configure a bit as an output, write a zero to that bit position in I/O address F874 hex. To output data on Port 3, write the data to I/O address

F872 hex. When used as inputs, these pins can also be configured to generate processor interrupts.

- P3PIN: F870h, Port Pin Status Register (read only), bits 0-5
- P3LTC: F872h, Port Latch Register, bits 0-5
- P3DIR: F874h, Port Direction Register, bits 0-5, 0 for output, 1 for input or open drain output.
- P3CFG: F824h, Port Configuration Register, bits 0-5 low, route P3.0-P3.5 to chip pins.

Asynchronous Serial (COM) Ports

The Flashlite has 2 serial ports, COM1 and COM2. Both ports are internal to the 386Ex and are compatible with the UARTs on a PC and the National Semiconductor 16C450 UART. The maximum data rate is 115k Baud.

COM1 is wired as Data Terminal Equipment (DTE) for connection to a peripheral such as a modem. This is a full function RS-232 port implementing all of the handshaking and control lines with the exception of the Ring Indicator input. See Table 2i for the connector wiring. The UART base address is at I/O location 3F8h and can be configured to use IRQ 4.

COM2 is the default console and is wired as Data Communications Equipment (DCE) for direct connection to a computer or terminal. This port is software configurable as a 3 wire RS-232 port implementing RxD and TxD or as a half duplex RS-485 port. See Table 2j for the connector wiring. The UART base address is at I/O location 2F8h and can be configured to use IRQ 3.

The following table shows the UART configuration and control registers. Please refer to the Intel 386Ex data sheet for more information on the serial ports and their configuration.

The DATA and IER registers also hold the baud rate divisor. When the high bit of the LCR (DLA) is set, the divisor value can be written to DATA and IER. DATA contains the low byte and IER contains the high byte. To determine the required divisor, divide 115200 by the required baud rate. Program the divisor with the nearest integer value. When access to the divisor value is no longer required, clear the DLA bit.

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	7	6	5	4	3	2	1	0
Base	Receive/Transmit Holding Register / Divisor Latch Low (DATA)							
	Data In, Data Out							
Base+1	Interrupt Enable Register (IER)							
	0	0	0	0	Modem Status	Receive Line Status	Transmit Buffer Empty	Receive Buffer Full
Base+2	Interrupt Identification Register / Divisor Latch High (IIR)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Interrupt Source 00=Modem Status 01=Transmit Buffer Empty 10=Receive Buffer Full 11=Receiver Line Status	Interrupt Pending (0=Pending)	
Base+3	Line Control Register (LCR)							
	Divisor Latch Access	Send Break	Parity 000=None, 001= Odd, 011=Even, 101=Mark, 111=Space			Stop Bits, 0=1, 1=2	Word Length, 00=5, 01=6, 10=7, 11=8	
Base+4	Modem Control Register (MCR)							
	0	0	0	Loop Back Test	Ext. Int. Enable	Out1	RTS	DTR
Base+5	Line Status Register (LSR)							
	Reserved	Transmit Register Empty	Transmit Buffer Empty	Break Interrupt	Framing Error	Parity Error	Overrun Error	Receive Buffer Full
Base+6	Modem Status Register (MSR)							
	DCD	RI	DSR	CTS	Δ DCD	Δ RI	Δ DSR	Δ CTS

Table 1: UART Registers

RS-485 Configuration

The COM2 port of the Flashlite can be configured and used for RS-485 communications. In order to avoid conflicts with DOS and the BIOS, it is first necessary to move the console to COM1. This is done using the utility program CON2COM1. Please note that COM1 (J6) is pinned out as DTE and you must use a null modem cable to connect it to a PC serial port.

To enable RS-485 operation (and disable RS-232) on COM2, clear bit 6 of I/O port F872 hex.

```
#define EN485_MASK 0xBF
#define EN485_REG 0xF872
outportb(EN485_REG, (inportb(EN485_REG) & EN485_MASK) );
// change to RS-485
```

Bit 0 of the PINCFG register must be set to allow control of the RS-485 transmit enable pin. The PINCFG register is located at I/O port F826 hex.

```
#define PINCFG 0xF826
outportb(PINCFG, (inportb(PINCFG) | 0x01) );
// connect TE control to chip pkg
```

The RTS line on COM2 is used to control the RS-485 transmitter. To transmit RS-485 data, set bit 1 of I/O port 2FC hex (mirrored at F8FC hex). To receive RS-485 data, clear bit 1. Note that the state of the chip pin is the inverse of the bit in the register (register=1, pin=0).

```
#define TX_MASK 0x02
#define TX_MASK_REG 0xF8FC
outportb(TX_MASK_REG, (inportb(TX_MASK_REG) | TX_MASK) );
    // enable transmitter
outportb(TX_MASK_REG, (inportb(TX_MASK_REG) & ~TX_MASK) );
    // disable transmitter
```

Two utility programs are available to aid RS-485 development. 485RX accepts RS-485 data and displays it on the console. 485TX accepts console data and sends it out the RS-485 port. The console must be switched to COM1 when using the utilities. These programs are installed on drive A:

Watchdog Circuitry

The Flashlite has two Watchdog protection features. The Hardware Watchdog is part of the reset control chip and the Watchdog Timer is a feature of the 386Ex processor chip.

The Hardware Watchdog requires that software write to a specific I/O port before its timer expires. If the timer expires, a system wide reset is issued and the board will restart. This is the preferred watchdog due to its ability to generate a hardware reset. JP2 must be installed to enable the Hardware Watchdog.

The BIOS will reset the Hardware Watchdog for approximately 5 seconds after power up giving the user application enough time to load. The user application must write a 0C hex to I/O location FF04 hex at least once every 1.6 seconds.

The Watchdog Timer is a counter that decrements once per processor clock cycle. When the counter reaches zero, the WDTOUT pin is asserted for 8 processor clock cycles. This signal can be internally routed to IR7 or externally jumpered to generate a Non-Maskable Interrupt (NMI). Software should periodically reload the counter register indicating that it is behaving properly.

The watchdog timer system has three modes: General Purpose, Software, and Bus Monitor. In General Purpose mode the counter can only be reloaded after it times out. This makes it difficult to use for system protection. The Software mode allows the countdown register to be reloaded before it times out. This allows protection against locked up software. The Bus Monitor mode is not applicable to the Flashlite hardware.

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To enable the watchdog in Software mode, use the following sequence:

1. Write the upper byte of the reload value to the WDTRLDH register (F4C0h).
2. Write the lower byte of the reload value to the WDTRLDL register (F4C2h).
3. Write two sequential words, F01Eh followed by 0FE1h, to the WDTCLR register (F4C8h).

Software will periodically repeat this sequence to refresh the counter and prevent it from generating an interrupt. The current value of the counter can be read from WDCNTH and WDCNTL at F4C4h and F4C6h. Once enabled in Software mode, the timer can not be disabled.

The watchdog is active on power up, defaults to general purpose mode and the counter has an initial value of 3FFFFFF hex. The counter can be disabled by setting bit zero of the WD TEN register at F4CAh. The Watchdog output is normally disabled by jumper JP3. If the watchdog is required, JP1 pins 1 and 2 should be shorted. Please refer to the Intel 386EX Embedded Microprocessor User's Manual for more information.

DiskOnChip 2000

M-Systems' DiskOnChip 2000 is a new generation of high performance single-chip Flash Disk. The DiskOnChip 2000 has become the standard Flash Disk module for Embedded Single Board Computers. The DiskOnChip MD2000 is a Flash Disk in a standard 32-pin DIP package that has built-in TrueFFS (True Flash File System) technology, allowing full read/write disk emulation. TrueFFS provides hard disk compatibility at both the sector and file level. 2, 4, 8, 12, 24, 40, 72 and 144 Mbyte capacity drives are available. Drives larger than 32Mbytes will require partitioning for use with XDOS.

DiskOnChip expansion is only supported on the Flashlite with 512K RAM / 512K Flash. Install the DiskOnChip module in the memory expansion socket U1. Note the location of pin 1. Set the memory type jumper (JP9) for Flash memory. If the DiskOnChip is installed and functioning, there will be an installation message that is displayed during the boot process and a C: drive will be available to DOS.

```
Bios Version 3.2g for Flashlite 386Ex with 256k or 512k Ram  
DOC Socket Services - Version 0.2  
(C) Copyright 1992-1996, M-Systems Ltd.
```

```
TrueFFS-BIOS -- Version 3.3.7 for DiskOnChip 2000 (V1.10)  
Copyright (C) M-Systems, 1992-1998
```

```
DOS Version 3.3c for JK microsystems Flashlite  
(C) HBS Corp and JK microsystems 1991-1999
```

```
B:\>
```

Jumpers

JP1 - Not Used

This jumper jumper is not used.
Default position: Open, no jumper fitted.

JP2 - Hardware Watchdog Enable

This jumper enables the Hardware Watchdog. If the Hardware Watchdog is required, JP2 pins 1 and 2 should be shorted.
Default position: Open, Hardware Watchdog disabled.

JP3 - Watchdog Non-Maskable Interrupt (NMI) Enable

This jumper connects the 386Ex watchdog signal to the processor NMI. If the watchdog is required, JP1 pins 1 and 2 should be shorted.
Default position: 2-3, Watchdog NMI disabled.

JP4 - Not Used

This jumper is not used.
Default position: Open, no jumper fitted.

JP5 - Power Fail Detect

This jumper connects the power fail detection circuitry to Port B pin 3. When this jumper is installed, Port B pin 3 will be driven high when the raw DC input voltage to the board is less than 8 volts.
Default position: Open, no jumper fitted.

JP6/JP12 - Boot Location

These jumpers allows the board to boot from the expansion socket. This is useful when performing field updates of the on-board Flash memory or when using an operating system other than DOS. Short JP6 pins 1-2 and JP12 pins 2-3 to boot from the on-board memory or jumper JP6 pins 2-3 and JP12 pins 1-2 to boot from the expansion socket.
Default position: JP6 pins 1-2 and JP12 pins 2-3, Boot from on-board flash.

JP7 - PLC Bus Vcc

This jumper connects Vcc to the PLC Bus (J14) connector when installed.
Default position: 1-2, Vcc available on PLC Bus (J14).

JP8 - SRAM Power Select

This jumper allows the SRAM contents to be maintained by the on-board battery when power fails. Jumper pins 1-2 for battery backup, pins 2-3 for Vcc power.
Default position: 2-3, SRAM does not have battery backup.

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JP9 - Socket Memory Type

These jumpers configure the memory type to be used in the expansion socket. Jumper pins 1-2 and 3-4 when using Flash or DiskOnChip, jumper 2-3 and 4-5 when using SRAM.

Default position: 1-2 and 3-4, Flash installed in expansion socket.

JP10 - Bus IRQ 3/5 Select

This jumper selects which IRQ is available on J13 pin 15. Jumper pins 1-2 to select IRQ5, jumper pins 2-3 to select IRQ3.

Default position: 1-2, IRQ5 on Extended Bus.

JP11 - Bus IRQ 4/6 Select

This jumper selects which IRQ is available on J13 pin 17. Jumper pins 1-2 to select IRQ6, jumper pins 2-3 to select IRQ4.

Default position: 1-2, IRQ6 on Extended Bus.

JP13 - PLC Bus Power

This jumper allows unregulated input power to be routed to the PLC Bus (J14, pin 4). Install this jumper to route power to the bus.

Default position: Open, Raw power not connected to PLC Bus.

Cables and Connectors

The following tables show the connector pin and signal name for each pin. For some pins, the signal direction is also shown.

NOTE: N/C indicates no connection and PULLUP indicates a 1k ohm pullup resistor to Vcc. Outputs refer to signals driven by the board and received by a peripheral. Inputs are driven by a peripheral and received by the board.

J1	Power
7-34 VDC	1
RESET/	2
GND	3

Table 2a: Power Pinout

J4	Power
7-34 VDC	1
GND	2

Table 2b: Power Pinout

J3	Power
SPKR	1
AUX	2
GND	3
VCC	4

Table 2c: Speaker Pinout

J5	RS-485
DATA +	1
GND	2
DATA -	3

Table 2d: RS-485 Pinout

J2		Port A & B	
GND	1	2	VCC
GND	3	4	VCC
GND	5	6	STXCLK/
GND	7	8	SRXCLK/
SSIORX/	9	10	SSIOTX/
PA.7	11	12	PB.7
PA.6	13	14	PB.6
PA.5	15	16	PB.5
PA.4	17	18	PB.4
PA.3	19	20	PB.3
PA.2	21	22	PB.2
PA.1	23	24	PB.1
PA.0	25	26	PB.0

Table 2e: Port A & B Pinout

J14		Port C / PLC Bus	
GND	1	2	VCC
N/C	3	4	DCIN
PD.3 (STB/)	5	6	GND
PD.2 (A3)	7	8	GND
PD.1 (A2)	9	10	GND
PD.0 (A1)	11	12	GND
PC.6 (D6)	13	14	PC.7 (D7)
PC.4 (D4)	15	16	PC.5 (D5)
PC.2 (D2)	17	18	PC.3 (D3)
PC.0 (D0)	19	20	PC.1 (D1)
PE.2 (WR/)	21	22	PE.3 (LCD)
PE.1 (RD/)	23	24	PE.0 (A0)
VCC	25	26	GND

Table 2f: Port C Pinout

J7		Port D & E	
PD.0	1	2	PD.1
PD.2	3	4	PD.3
PE.0	5	6	PE.1
PE.2	7	8	PE.3
GND	9	10	VCC

Table 2g: Port D & E Pinout

J12	Port F
PF.4	1
PF.5	2
PF.6	3
PF.7	4
GND	5
VCC	6
IRQ5	7
IRQ6	8

Table 2h: Port F Pinout

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COM1 is configured as a DTE port, and is generally used to communicate with a peripheral device. COM2 is configured as a DCE port, generally being used to connect the Flashlite to another computer. A 10 pin dual row header to 9 pin to D-type connector may be required to connect the Flashlite to a peripheral or computer. See the tables below for connector pinouts.

J6		COM1:	
DCD (in)	1	2	DSR (in)
RxD (in)	3	4	RTS (out)
TxD (out)	5	6	CTS (in)
DTR (out)	7	8	N/C
GND	9	10	N/C

Table 2i: COM1 Pinout

J11		COM2:	
PULLUP	1	2	N/C
TxD (out)	3	4	PULLUP
RxD (in)	5	6	PULLUP
N/C	7	8	PULLUP
GND	9	10	N/C

Table 2j: COM2 Pinout

J10		Host Parallel Port	
STROBE/	1	2	AUTO/
D7	3	4	ERROR/
D6	5	6	N/C
D5	7	8	SLCT IN/
D4	9	10	GND
D3	11	12	GND
D2	13	14	GND
D1	15	16	GND
D0	17	18	GND
ACK/	19	20	GND
BUSY/	21	22	GND
PE/	23	24	GND
SLCT	25	26	GND

Table 2k: Host Parallel Port Pinout

J8		JTAG	
RD/	1	2	TAPIN
WR/	3	4	TAPOUT
PULLUP3	5	6	TAPCLK
CS1/	7	8	TAPMODE
CS0/	9	10	RESET/
UCS/	11	12	GND

Table 2l: JTAG Port Pinout

J9		Processor Bus	
GND	1	2	VCC
GND	3	4	VCC
MREQ/	5	6	D7
MSTB/	7	8	D6
IOSTB/	9	10	D5
RW/	11	12	D4
REFRQ/	13	14	D3
RESET/	15	16	D2
IORD/	17	18	D1
IOWR/	19	20	D0
A9	21	22	A19
A8	23	24	A18
A7	25	26	A17
A6	27	28	A16
A5	29	30	A15
A4	31	32	A14
A3	33	34	A13
A2	35	36	A12
A1	37	38	A11
A0	39	40	A10

Table 2m: Processor Bus Pinout

J13		Extended Bus	
GND	1	2	IRQ9
LBA/	3	4	D15
BS8/	5	6	D14
IO/	7	8	D13
W-R/	9	10	D12
D-C/	11	12	D11
ADS/	13	14	D10
IRQ 3/5	15	16	D9
IRQ 4/6	17	18	D8
A24	19	20	A23
A22	21	22	A21
A20	23	24	A19
VCLK	25	26	GND

Table 2n: Extended Bus Pinout

Pin 1 of a connector can be identified in several ways. Pin one has a square PCB pad and the others are round. This should be visible on the bottom of the PCB. Pin one will also be identified on the board silkscreen with a '1' and/or a dot. Dual row headers have ODD numbered pins on one side and EVEN numbered pins on the other. The dual row header numbering scheme follows the numbering of an IDC style ribbon cable. This numbering may not be identical to connectors with discrete wires. Use caution when connecting cables to the Flashlite.

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Software

Supported PC BIOS Functions

The Flashlite BIOS supports the following functions (software interrupts) common to PC compatible computers. Please refer to a DOS/PC reference for more information on DOS and BIOS software interrupts.

Int 10h, Video Driver, Functions 9 and Eh
Int 11h, Get Equipment Configuration
Int 12h, Get Memory Size
Int 13h, Disk Driver, Functions 0-4
Int 14h, Serial Port Driver, Functions 0-3
Int 16h, Keyboard Driver, Functions 0 and 1
Int 19h, Boot System
Int 1Ch, Hook Timer Tick Interrupt
IRQ0 / Int 8, Timer Tick Interrupt

Interrupts

Working with interrupts within the PC architecture can be a bit confusing. The following information should clarify some of the issues, but it is not a substitute for a detailed DOS/PC programming reference.

The PC architecture has a 1Kbyte Interrupt Vector Table located at 0000:0000. This table holds the 4byte address of each Interrupt Service Routine (ISR) providing a total of 256 interrupts. Most of the interrupts are software interrupts. Software interrupts provide essential services in a 'known' location. Hardware interrupt requests have an associated interrupt number and ISR in the vector table. Refer to a DOS/PC reference for more information on software interrupts.

The numbering of hardware interrupts is the largest point of confusion when working with interrupts on the Flashlite. The 386Ex processor interrupt pins are referred to as INTx in the Intel documentation. PC programmers are familiar with IRQ (Interrupt Request) numbers and the interrupt numbers also referred to as INT numbers. The correlation of all these numbers is critical when using interrupts. The table below identifies the IRQ, 386Ex INT number, function on a standard PC, function on the 386Ex and the interrupt number. You will notice a large gap in interrupt numbers between IRQ7 and IRQ8. This is due to the implementation of two cascaded interrupt controllers and the PC legacy. IRQ0-7 are on the first controller, found in the original PC/XT. IRQ8-15 are on the second controller implemented in the PC/AT. IRQ2 notifies the system when an IRQ is triggered on the secondary controller. Table entries without a 386Ex INT listed are not available on the package pins of the 386Ex.

IRQ	386Ex INT	PC Function	386Ex Function	Int. No. (hex)
IRQ0		System Timer	TCU OUT0	08
IRQ1	INT0	Keyboard	P3.2	09
IRQ2		Cascade		0A
IRQ3	INT8	COM2	SIO1 INT	0B
IRQ4	INT9	COM1	SIO0 INT	0C
IRQ5	INT1		P3.3	0D
IRQ6	INT2	Floppy Disk	P3.4	0E
IRQ7	INT3	Parallel Port	P3.5	0F
IRQ8	INT4	Real Time Clock		70
IRQ9	INT5	IRQ2 (redirected)		71
IRQ10			TCU OUT1	72
IRQ11			TCU OUT2	73
IRQ12	INT6	Mouse		74
IRQ13		Math Coprocessor		75
IRQ14	INT7	Hard Disk		76
IRQ15			WDTOUT	77

Table 3: Hardware Interrupts

Each Programmable Interrupt Controller (PIC) has several control registers and commands, most of which are configured by the BIOS and should not require modification in most applications. The primary PIC is located at I/O address 20 hex and the secondary controller is at I/O address A0 hex.

The first command of interest is the Operation Control Word (OCW). Located at $\text{BASE}+1$, it is the mask byte for the interrupts in that controller. Masked IRQ's have a one in the corresponding bit location, enabled interrupts have a zero. Be sure to only change the mask bits for IRQ's handled by your program. For example, to enable IRQ 4:

```
outportb(0x21, (inportb(0x21) & 0xEF);
```

The other instruction used is the End Of Interrupt (EOI). This instruction is sent to the appropriate PIC after an interrupt has been processed. The EOI is instruction 20 hex and is sent to the BASE address of the controller, for example:

```
outportb(0x20, 0x20);
```

When servicing an interrupt on the secondary controller (IRQ8-15), it is necessary to send an EOI to both controllers.

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Utilities

The Flashlite comes preloaded with several utilities to aid system development. These utilities are located on drive A: of the Flashlite or the Utilities disk.

UP.COM

This utility facilitates uploading files to the Flashlite via the console port using the X-MODEM transfer protocol. The utility requires the user to supply the name of the incoming file. Unless otherwise specified, the file is placed in the active directory of the current drive. Be sure that B: is the current drive or a write-protect error will occur when UP tries to write to the read-only A: drive.

```
B:\>up
```

```
Upload file with X-MODEM Protocol
```

```
Usage: up file...
```

```
Version 2.0 for JK microsystems Flashlite V25 and 386Ex
```

```
B:\>up test.exe
```

```
Ready, start X-modem upload now,
```

```
Press CNTL-C to abort...
```

```
CCCC
```

```
B:\>
```

DOWN.COM

This utility facilitates downloading files from the Flashlite via the console port using the X-MODEM transfer protocol. The utility requires the user to supply the name of the file to transmit.

```
B:\>down
```

```
Download file with X-MODEM Protocol
```

```
Usage: down file...
```

```
Version 1.0 for JK microsystems SBC products
```

```
B:\>down test.exe
```

```
Ready, start X-modem download now,
```

```
B:\>
```

FORMAT.COM

If it becomes necessary to reformat the B: drive, FORMAT provides this function. CAUTION, all information on the drive will be lost during the formatting process.

```
B:\>format
Flashlite FLASH Drive Format Program -Version 3.0
System will reboot after successful format...
```

```
Press 1 to initialize Drive B as 418 KB disk
Press ESC to exit with no changes
```

```
>1
Flash Drive is now formatted
Rebooting system...
```

EDIT.COM

A simple line editor is included to allow quick creation and modification of batch files or other text files. EDIT is similar to Microsoft's EDLIN provided in earlier versions of MS-DOS. It allows list, insert, delete, and modify. Upon exit, a backup of the original file is created (filename.BAK) and the edits are saved. If a backup file with the same name already exists, it is overwritten. A list of commands and their usage is available by entering 'h' at the edit prompt (>>). The name of the file to edit must be supplied following the command EDIT on the command line.

```
B:\>edit test.bat
FlashLite Line Editor v1.0
Enter h for help
```

```
New File: test.bat
>> i
0: @echo Batch file being processed...
   1: mytsr
   2: myapp
   3: ^Z
>> l
0: @echo Batch file being processed...
   1: mytsr
->   2: myapp
>> q
Save before exit (Y,n): y
File Saved
B:\>
```

DOS

JK microsystems' controllers use XDOS, a compact operating system for embedded applications. The XDOS command structure is nearly identical to MS/PC DOS version 3.3. The switches for the DIR command have been changed and expanded. XDOS does not support redirected input or output with the use of < and >, but does support pipes (|). None of the external DOS commands are provided due to storage constraints. XDOS does not support installable file system functions.

XDOS Command Reference

In the list below, XDOS commands are followed by a function description and their format including available parameters and switches. Items in boldface type must be entered. Capitals or lowercase letters may be used. Items in italics are parameters. Those in boldface italics must be entered, those in [] are optional. All switches are optional. They are shown as [/X]. Spaces and punctuation are to be included. An ellipsis ... following items means that you may repeat the items as often as needed. Do not enter the ellipsis or the square brackets. Most XDOS commands allow the use of wildcards in filenames and extensions. When wildcards (?=one character, *=any character or characters) are used, the command is executed once for each matching file.

Common parameters are:

[d:]	drive specification - a letter followed by a colon (:), e.g. A:; if no drive is specified, the default drive is used.
[path]	the path DOS must take in traveling from one directory to another; directory names are separated by a backslash (\).
[filename]	up to 8 characters used to name a file.
[.ext]	a three character extension may be added to a filename; an extension is separated from a filename by a period.

CD / CHDIR

Function: Changes the current directory
Format: **CD** or **CHDIR** [[d:]path]

COPY

Function: Copies a file, combines two or more files into one file, or transfers data between files and DOS devices
Format: **COPY** [d:][path]filename[.ext][switches]
 [+[d:][path]filename[.ext]][switches]
 [d:][path][filename[.ext]][switches]
Switches: /V - verify the contents of new file
 /A - copy file in ASCII format
 /B - copy file in binary format

DATE

Function: Displays or changes the current DOS date.
Format: **DATE** [*mm-dd-yyyy*]

DEL / ERASE

Function: Deletes (erases) one or more files from a disk
Format: **DEL** or **ERASE** [*d:*][*path*][*filename*.[*ext*]]

DIR

Function: Lists directory entries
Format: **DIR** [*d:*][*path*][*filename*.[*ext*]][*switches*]
Switches:
/a - display file attributes
/b - sort by file size (in bytes)
/d - sort entries by date and time
/f - display entries by alphabetic file name order
/n - display entries in directory order (do not sort)
/s - include system and hidden files in output
/h - display this Help screen (any invalid key)

MD / MKDIR

Function: Creates a subdirectory
Format: **MD** or **MKDIR** [*d:*]*path*

PATH

Function: Specifies directories that DOS is to search when trying to locate executable files
Format: **PATH** [[*d:*]*path*[:[*d:*]*path* ...]]

PROMPT

Function: Sets the DOS system prompt
Format: **PROMPT** [*text*]
Text: Resulting Character(s):
\$t The current time stored by DOS
\$d The current date stored by DOS
\$p The current directory
\$v The version of DOS being used
\$n The default drive
\$g The character >
\$l The character <
\$b The character |
\$q The character =
\$\$ The character \$
\$_ Carriage return plus line feed

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REN

Function: Renames a file

Format: **REN** [*d:*][*path*]*filename*[.ext] *filename*[.ext]

RD / RMDIR

Function: Deletes a subdirectory

Format: **RD** or **RMDIR** [*d:*]*path*

TIME

Function: Displays or changes the current DOS time

Format: **TIME** [*hh:mm:ss.xx*]

TYPE

Function: Display the contents of a file

Format: **TYPE** [*d:*][*path*]*filename*[.ext]

VER

Function: Displays the DOS version number

Format: **VER**

VOL

Function: Displays the volume label of specified drive

Format: **VOL** [*d:*]

QuickBASIC Console I/O

Some of the code produced by Microsoft QuickBASIC and QuickBASIC Professional compilers does not execute properly on the Flashlite. In the case of console I/O, we believe that QuickBASIC is generating code for specific hardware and software not present on the Flashlite controller.

There are two problems with console I/O. The first is that a PRINT statement will not send output to the console port. To output text to the console, open "cons:" as a file and print to it.

```
OPEN "o", 1, "cons:"
PRINT #1, "This is a test of Console output"
```

The second problem is that an INPUT statement will not echo data entered by the user. To work around this problem, use the line input function listed below.

```
rem    linein returns the echoed string of text linein$ from
rem    the console.
rem    If you need the text in the form of a number, use
rem    VAL(linein$) to convert the string to a number
```

```
linein:
    linein$ = ""
linemore:
    a$ = INKEY$
    IF a$ = "" THEN GOTO linemore
    IF a$ = CHR$(13) THEN GOTO linedone
    IF a$ <> CHR$(8) THEN GOTO getchar
    PRINT #1, CHR$(8); CHR$(32); CHR$(8);
    linein$=left$(linein$, (len(linein$)-1))
    GOTO linemore
getchar:
    PRINT #1, a$;
    linein$ = linein$ + a$
    GOTO linemore
linedone:
    PRINT #1, ""
    RETURN
```

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Specifications

Supply Voltage:	7 - 34 V DC, unregulated
Supply Power:	1.8 Watts (nominal)
Supply Current:	260mA @ 7 Volts input 150mA @ 12 Volts input 75mA @ 24 Volts input
Operating Temperature:	-20 to +85 °C
Humidity:	5 - 90 % non-condensing

I/O Port A,B & C Characteristics:

Symbol	Parameter	MIN	MAX	Units	Condition
V _{IL}	Input Low		0.8	V	
V _{IH}	Input High	2.0		V	
V _{OL}	Output Low		0.4	V	I _{OL} = 2.5mA
V _{OH}	Output High	3.0		V	I _{OH} = -2.5mA

I/O Port D & E Characteristics:

Symbol	Parameter	MIN	MAX	Units	Condition
V _{IL}	Input Low	-0.5	0.8	V	
V _{IH}	Input High	2.0	V _{CC} +0.5	V	
V _{OL}	Output Low		0.45	V	I _{OL} = 12mA
V _{OH}	Output High	2.4		V	I _{OH} = -4mA

I/O Port F Characteristics:

Symbol	Parameter	MIN	MAX	Units	Condition
V _{IL}	Input Low	-0.3	0.8	V	
V _{IH}	Input High	2.0	V _{CC} +0.3	V	
V _{OL}	Output Low		0.45	V	I _{OL} = 8mA
V _{OH}	Output High	V _{CC} -0.5		V	I _{OH} = -8mA

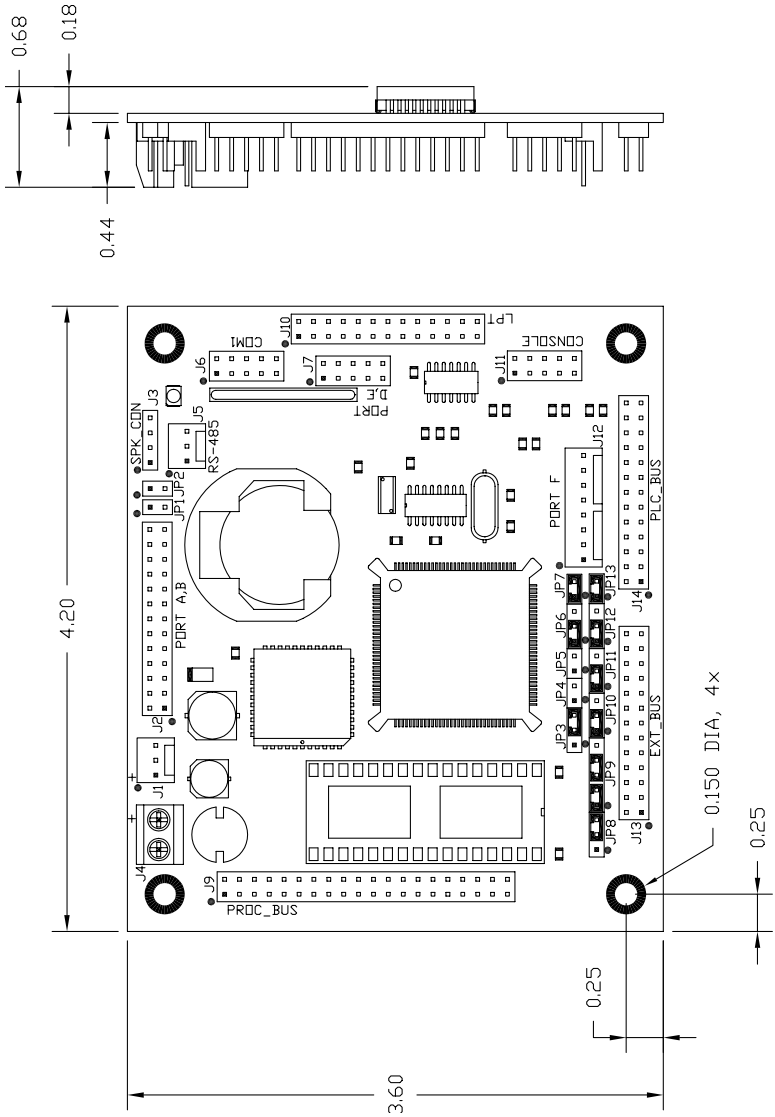
Mating Connectors:

Connector	Mfg	MFG P/N	JK micro P/N
J6, J7, J11	Molex	22-55-2101	
	Oupiin	4072-2X05H	28-0030
J2, J10, J14	Molex	22-55-2261	
	Oupiin	4072-2X13H	28-0031
Pins	Molex	16-02-0096	
	Oupiin	404-PIN-10K	28-0033
J1, J5	Molex	22-01-2031	28-0012
J12	Molex	22-01-2081	28-0037
Pins	Molex	08-50-0114	28-0013

Mechanical:

Dimensions	4.20" x 3.60" (106.7 mm x 94.1 mm)
Weight	2.9oz (82.2 gm)

Specifications



Flashlite 386Ex User's Manual

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